Microwave Power GaAs FET Amplifiers

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Abstract—**The development of broad-band microwave amplifiers using state-of-the-art GaAs power FET's covering the 6–12-GHz frequency band is presented. A unique circuit topology incorporating an edge-coupled transmission line section for both impedance matching and input/output dc blocking is described. The microstrip circuit design of an *X*-band 1-W 22-dB-gain GaAs FET amplifier is also discussed. Microwave performance characteristics such as intermodulation, AM-to-PM conversion, and noise figure are included.**

I. Introduction

HIGH-POWER high-efficiency amplification of microwave power using GaAs FET's has been demonstrated recently for operating frequencies in *C*, *X*, and *Ku* band [1], [2]. Single-stage and multistage amplifiers with 1-W output power have already been reported in the *C*-band frequencies with a bandwidth of 500–600 MHz [3], [4]. Although broad-band small-signal low-noise GaAs FET amplifiers are commercially available for receiver applications from *C*- through *X*-band frequencies, the output powers of such amplifiers are generally limited to a level of 5–10 mW. With the advent of GaAs power FET's it appears to be possible to design solid-state power amplifiers for active-element phased-array radars, communications, and ECM systems. The feasibility of using the state-of-the-art GaAs power FET in the design of microstrip amplifiers operating in the *C*- and *X*-band frequencies is described.

In Section II the techniques for active device evaluation, including the small- and large-signal *S*-parameter measurements, are discussed. Section III describes a unique circuit topology that is capable of broad-band impedance matching, covering an octave bandwidth (6–12 GHz). Experimental results for several single-stage broad-band amplifiers are also presented. Finally, in Section IV the microwave performance of multistage power FET amplifiers is covered. The possibility of using an IMPATT amplifier as the output stage in a hybrid FET/IMPATT amplifier configuration is also demonstrated in Section IV.

II. RF Device Characterization

To achieve optimum amplifier performance, especially in the design of broad-band microwave amplifiers, it is essential to characterize the RF properties of the active device. For the design of the FET amplifiers discussed in this paper the FET chip was characterized in terms of its two-port *S* parameters. Small-signal *S*-parameter measurements were made using an HP 8743 network analyzer. For characterization at large-signal levels the HP 8742 reflection test unit together with the network analyzer were used to qualitatively establish the trend in the *S* parameters under high output-power conditions.

The GaAs FET's used in these amplifiers are similar to those reported elsewhere [2]. A single-cell FET consists of four 150-μm (gate width) Schottky-barrier gate stripes with each stripe having a gate length of 1.5–2 μm. Up to four cells can be connected in parallel on a single FET chip to provide a total gate width of 2400 μm for increased power-output requirements. The chip is mounted upright on a gold-plated copper carrier. This same carrier is used for both device characterization and actual amplifier construction. In this way, the effects of parasitic reactances due to the mounting structure will be nearly the same in both cases. The FET copper carrier is clamped between two gold-plated copper blocks which serve as carriers for the microstrip input and output circuits. For *S*-parameter measurements these input and output microstrip circuits are simply 50-Ω lines fitted with input and output OSM connectors.

Table I shows a typical set of the measured small-signal *S* parameters for a one-cell FET measured at 500-MHz intervals from 7 to 12 GHz. Bias conditions for such a device are as indicated. Also shown are the associated maximum stable gain (MSG), the Rollett's stability factor *K*, and the maximum available gain (MAG). It is interesting to note that the MAG follows very nearly the fundamental 6-dB/octave gain rolloff characteristic expected for such microwave devices. Since the product of the forward and reverse transmission parameters $S_{12} \cdot S_{21}$ is a factor of 5–10 times smaller in magnitude than either $|S_{11}|$ or $|S_{22}|$ in the frequency range shown, the input and output impedances of this FET device are relatively insensitive to varying source and load conditions, and can be approximated by the impedances corresponding to S_{11} and S_{22}, respectively.

The phases of both S_{11} and S_{22} retard with increasing frequency, and the phase of S_{11} is such that the input susceptance changes from capacitive to inductive in the frequency range shown. This behavior is due to the short ($\sim$ 10-mil) input and output 1-mil wires which are considered here as part of the device and whose inductive reactances are included in the measured *S* parameters.

Measurements of the *S* parameters for multicell devices have also been made. One of the main differences between one-cell and multicell devices is that the input and output impedance levels drop by roughly a factor equal to the

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TABLE I
MEASURED *S* PARAMETERS OF A SINGLE-CELL (600-μm GATE WIDTH) GaAs POWER FET FOR COMMON SOURCE OPERATION

FREQ. (GHZ)	MSG (DB)	K	MAG (DB)	$\|S_{11}\|/\theta°$	$\|S_{12}\|/\theta°$	$\|S_{21}\|/\theta°$	$\|S_{22}\|/\theta°$
7.00	12.0	1.30	8.7	0.770/-138.	0.075/ 22.	1.180/ 55.	0.610/ -78.
7.50	11.8	1.31	8.4	0.750/-145.	0.080/ 24.	1.200/ 49.	0.630/ -66.
8.00	12.0	1.39	8.2	0.740/-149.	0.074/ 21.	1.160/ 42.	0.660/ -75.
8.50	11.4	1.40	7.6	0.700/-150.	0.087/ 21.	1.200/ 39.	0.660/ -64.
9.00	10.9	1.70	6.1	0.690/-155.	0.084/ 21.	1.040/ 32.	0.650/ -72.
9.50	11.0	1.88	5.6	0.640/-165.	0.083/ 21.	1.050/ 30.	0.650/ -71.
10.00	10.8	1.62	6.2	0.660/-170.	0.090/ 22.	1.070/ 25.	0.650/ -70.
10.50	10.3	1.63	5.7	0.660/-172.	0.100/ 21.	1.080/ 16.	0.605/ -72.
11.00	9.8	1.90	4.4	0.610/ 179.	0.110/ 20.	1.060/ 10.	0.520/ -82.
11.50	10.0	2.06	4.1	0.600/ 163.	0.108/ 12.	1.070/ -5.	0.470/-100.
12.00	9.5	1.85	4.2	0.660/ 173.	0.116/ 11.	1.040/ -3.	0.420/-105.

Bias: Gate Voltage =-1 V, Drain Voltage = 7 V
Drain Current = 60 mA

TABLE II
MEASURED *S* PARAMETERS OF A FOUR-CELL (2400-μm GATE WIDTH) GaAs POWER FET FOR COMMON SOURCE OPERATION

FREQ. (GHZ)	MSG (DB)	K	MAG (DB)	$\|S_{11}\|/\theta°$	$\|S_{12}\|/\theta°$	$\|S_{21}\|/\theta°$	$\|S_{22}\|/\theta°$
7.00	12.1	1.81	6.9	0.840/ 173.	0.048/ 26.	0.780/ 14.	0.640/-127.
7.50	11.6	1.37	7.9	0.880/ 175.	0.045/ 35.	0.650/ 13.	0.700/-137.
8.00	11.2	2.65	4.2	0.810/ 178.	0.045/ 50.	0.600/ 15.	0.710/-139.
8.50	10.2	1.62	5.5	0.840/ 178.	0.055/ 55.	0.570/ 4.	0.730/-135.
9.00	9.2	2.03	3.4	0.825/ 179.	0.059/ 49.	0.490/ 12.	0.730/-139.
9.50	9.2	2.64	2.1	0.795/-179.	0.058/ 50.	0.480/ 8.	0.720/-135.
10.00	8.7	1.98	3.1	0.790/-178.	0.067/ 55.	0.500/ 4.	0.740/-131.
10.50	8.0	1.40	4.2	0.816/ 180.	0.075/ 50.	0.470/ -2.	0.760/-132.
11.00	7.3	1.91	1.8	0.800/ 173.	0.077/ 54.	0.410/ -6.	0.750/-131.
11.50	7.2	1.73	2.2	0.750/ 164.	0.091/ 48.	0.480/ -9.	0.740/-124.
12.00	6.5	1.93	1.0	0.752/ 152.	0.091/ 53.	0.410/ -14.	0.760/-128.

Bias: Gate Voltage = -1 V, Drain Voltage = 7 V
Drain Current = 250 mA

number of cells. One of the results is that the magnitude of S_{11}, for example, increases, and for a four-cell device is about 0.82 at 9.5 GHz. The phase of S_{11} for a four-cell device decreases by about 15° at 9.5 GHz when compared to the corresponding one-cell device. This is due to the increase in the total gate capacitance of the multicell FET.

The magnitude of S_{22} for a four-cell FET is slightly larger than for a one cell and is about 0.74 at 9.5 GHz, while the phase is more retarded and equal to about $-135°$ at 9.5 GHz. The calculated MAG for the multicell devices is slightly less than for the corresponding one-cell FET's, with the difference being typically 1–2 dB. It is believed that these differences arise from the multicell interconnect scheme and the corresponding increase in parasitics. A complete set of measured *S*-parameter data for a four-cell device is shown in Table II. It is seen that the fluctuations in the calculated MAG are much more severe than in the corresponding data for a one-cell device. These fluctuations are mostly due to measurement error in the magnitudes of the *S* parameters and are more pronounced in the four-cell case because both $|S_{11}|$ and $|S_{22}|$ are closer to unity, i.e., the normalized (to 50 Ω) impedance levels are smaller for the four-cell case and are more difficult to measure accurately. More accurate measurements could be made by employing a carefully designed and characterized impedance transformer and performing the measurements at a lower impedance level.

For the design of matching networks suitable for FET power amplifiers it is necessary to characterize, at least qualitatively, the FET under high-power operation. To this end preliminary measurements have been made on the large-signal *S* parameters to determine 1) at what power

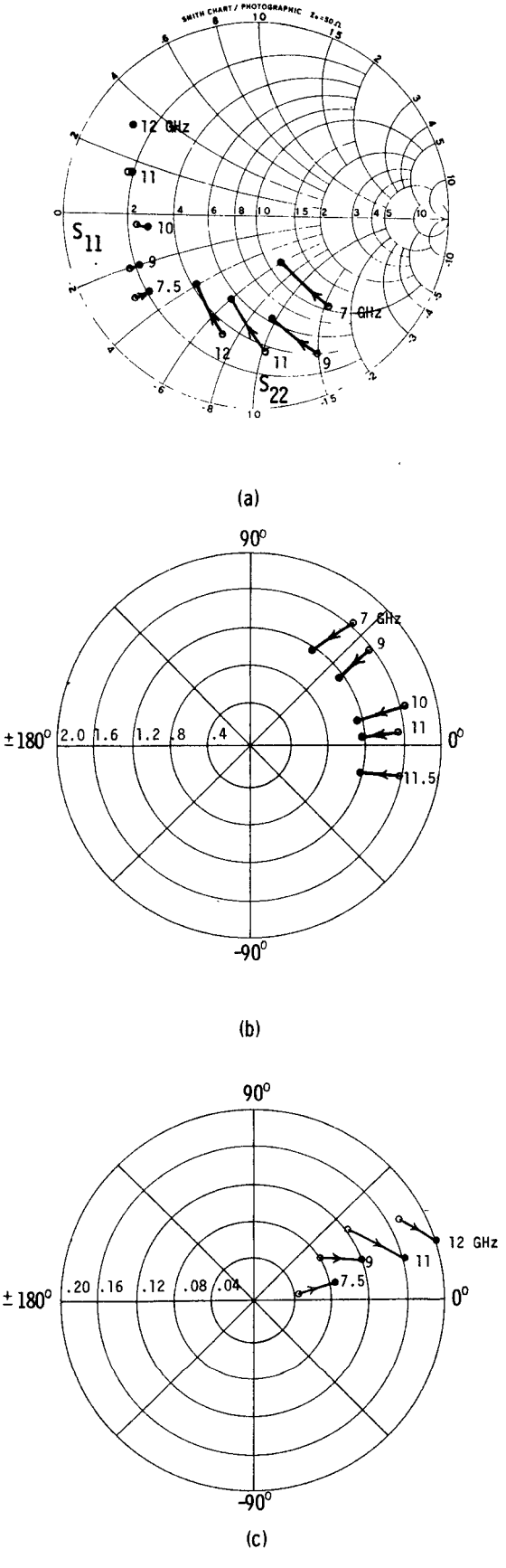


Fig. 1. Measured large-signal S parameters of a single-cell FET for common source operation. (a) S_{11} and S_{22}. (b) S_{21}. (c) S_{12}. Bias: $V_D = 7$ V, $V = -1$ V, $I_D = 81$ mA.

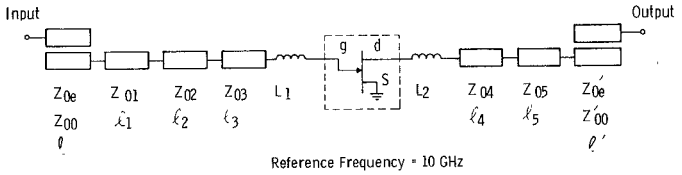
levels do the new S parameters start to deviate significantly from the small-signal values, and 2) when plotted on a Smith chart, in what direction do these deviations take place. For these measurements the HP 8742 reflection test unit, in conjunction with the HP 8410 network analyzer, was used to drive the FET at large-signal levels. For the measurement of S_{11} and S_{22} the 8742 was used in the usual manner as specified by the manufacturer for reflection measurements. The measurement of the large-signal transmission parameters S_{12} and S_{21} was accomplished by terminating the "reflected" port of the 8742, feeding the input signal to the FET from the "unknown" port, and by means of the HP 11605A flexible arm, connecting the output of the FET under test to the "test" port of the harmonic frequency converter of the 8410 network analyzer. The reference signal was obtained as usual from the 8742 and connected to the harmonic frequency converter. Precision attenuator pads were used to reduce the power to levels compatible with proper operation of the harmonic frequency converter.

The measurements were performed on a one-cell FET driven with a CW input power of up to 26 dBm. Fig. 1 shows the variation of S parameters with signal level at selected frequencies. For $|S_{11}|$ deviations from the small-signal values occurred at about 10 dBm with the greatest change occurring at the lower frequencies. At 7.5 GHz the magnitude decreased by about 13 percent at 26 dBm while at 12 GHz $|S_{11}|$ was virtually unaffected at the 26-dBm level. The phase of S_{11} was in all cases essentially the same as the small-signal value. S_{22} changed the most both in magnitude and phase, and deviations from the small-signal value also occurred at about the 10-dBm power level. At 26 dBm the magnitude of S_{22} decreased by as much as 51 percent at 7 GHz and 25 percent at 12 GHz. The phase also retarded from about 10° at the lower frequencies to about 25° at 12 GHz. The forward transmission parameter S_{21} changed very little in phase and decreased by about 25 percent in magnitude fairly uniformly across the frequency range of 7–12 GHz. Deviations from the small-signal values occurred at about 21 dBm of input power at 7 GHz and about 18 dBm at 12 GHz. Finally, the reverse transmission parameter S_{12} increased in magnitude and decreased in phase with the decrease in phase being more prominent at the higher frequencies. The increase in magnitude was about 58 percent at 7.5 GHz and about 20 percent at 12 GHz. At 7.5 GHz the phase of S_{12} decreased only slightly while at 12 GHz the phase decreased by about 15° from the small-signal value.

The aforementioned trends in the S parameters may be used as guidelines in modifying amplifier matching circuits which are designed on the basis of the small-signal S parameters, in order to achieve optimum amplifier performance at high power levels.

III. Broad-Band Single-Stage FET Amplifiers

The results of the S-parameter measurements presented in Section II have been used in conjunction with a computer optimization routine to generate the circuit elements of the matching networks for a number of single-stage broad-band



INPUT CIRCUIT

Frequency (GHz)	Z_{0e} (Ω)	Z_{00} (Ω)	ℓ (λ)	Z_{01} (Ω)	ℓ_1 (λ)	Z_{02} (Ω)	ℓ_2 (λ)	Z_{03} (Ω)	ℓ_3 (λ)	L_1 (nH)
6 - 10	137.0	40 0	0 27	51.0	0. 12	33 4	0 01	12.5	0. 10	0.27
8 - 12	137.0	40.0	0.20	50.0	0.09	33 0	0.05	12.5	0.09	0 15
6 - 12	137 0	40 0	0.31	40.4	0.07	35.1	0.08	12 8	0 05	0. 16

OUTPUT CIRCUIT

Frequency (GHz)	L_2 (nH)	Z_{04} (Ω)	ℓ_4 (λ)	Z_{05} (Ω)	ℓ_5 (λ)	Z_{0e} (Ω)	Z'_{00} (Ω)	ℓ' (λ)
6 - 10	1.30	28 9	0. 18	50.0	0 05	137 0	40 0	0 38
8 - 12	0. 84	38.5	0.25	50.0	0.02	137 0	40.0	0 32
6 - 12	1 03	32 8	0. 12	53.0	0 09	1370	40 0	0 30

Fig. 2. A circuit topology for broad-band FET amplifier design. The optimized circuit element values are shown in the tables for the 6–10-, 8–12-, and 6–12-GHz amplifiers.

amplifiers with prescribed gain responses. It is well known that the intrinsic FET's generally exhibit a characteristic gain rolloff with increasing frequency (~ -6-dB/octave). To maintain a constant gain across the design frequency band, the matching network must be designed for maximum gain at the highest frequency of interest [5], [6]. Mismatches must be provided to compensate for the increase in the intrinsic gain of the FET when the frequency is decreased. Either a reflective or an absorptive technique can be used to provide the required gain taper. In this work, reflective mismatches, i.e., input and output VSWR, have been used to provide the gain compensation.

The optimization of impedance matching networks for transistor amplifiers operating at microwave frequencies has received increased attention due to the availability of high-performance GaAs FET and silicon bipolar transistors at *X*-band frequencies [2], [7]. Fig. 2 shows a unique circuit topology that has been used successfully for broad-band amplifier design covering different frequency ranges and widely different device *S* parameters. The input circuit consists of an edge-coupled transmission line section, three impedance transformers, and a lumped inductance close to the device. The output circuit is essentially the same as the input circuit except for the use of two transformers and the differences in line lengths and characteristic impedances to account for the different impedance characteristics of the gate and drain of the GaAs FET. In addition to serving the impedance matching function, the edge-coupled line section can also be used as a dc block, thus eliminating the requirement for a discrete dc blocking capacitor. This dc blocking scheme has been used successfully in the designs of *X*- and *Ku*-band IMPATT/Read amplifiers [8], [9]. The required lumped inductances can be realized with the bondwire inductances of the gate and drain.

A generalized computer routine for computer-aided design of linear electronic circuits has been used for the design of broad-band FET amplifiers using the *S* parameters

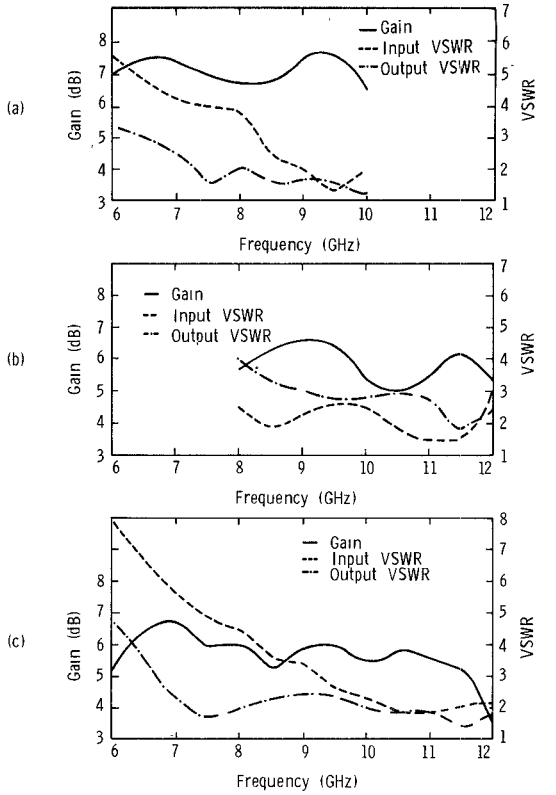


Fig. 3. Gain-frequency response and VSWR characteristics of three wide-band single-cell FET amplifiers with the circuit element values shown in Fig. 2. (a) 6–10 GHz. (b) 8–12 GHz. (c) 6–12 GHz.

discussed in Section II. The inputs to the computer program are the 2-port frequency-dependent *S* parameters and the appropriate circuit topology such as that shown in Fig. 2. In addition, the circuit performance criteria and physically realizable constraints on the circuit elements are specified. The output includes optimized values for the parameters of the circuit topology along with the performance characteristics of the optimized circuit.

Wide-band amplifiers covering the 6–10, 8–12, and 6–12-GHz frequency ranges have been designed, using the computer program described previously for a single-cell GaAs FET with a gate width of 600 μm. The tables in Fig. 2 show the optimized circuit parameters for amplifiers designed for different frequency ranges of operation. From the tables it is seen that the circuit elements are within the physically realizable limits of microstrip circuits using alumina substrates. For the edge-coupled filter section, the required even- and odd-mode impedances correspond to a width-to-height ratio (w/h) of 0.2 and a spacing-to-height ratio (s/h) of 0.1, using an alumina substrate with a dielectric constant of $\sim$ 9.6. A characteristic feature of the circuit topology shown in Fig. 2 is that, in most cases, only very short lengths of transmission lines are required. This has the advantages of minimizing the circuit losses and providing a compact amplifier design. Fig. 3 shows the gain-frequency responses of the three amplifiers corresponding to the circuits shown in Fig. 2. The input and output VSWR variations as a function of frequency are also shown with each of the amplifier gain responses. It is noted that the

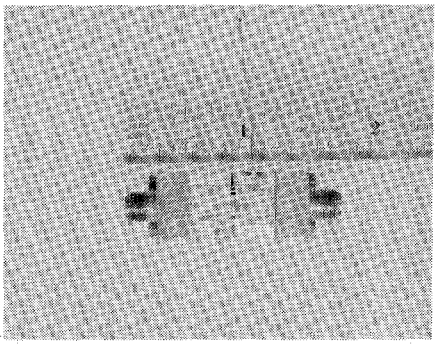


Fig. 4. A simple microstrip single-cell FET amplifier.

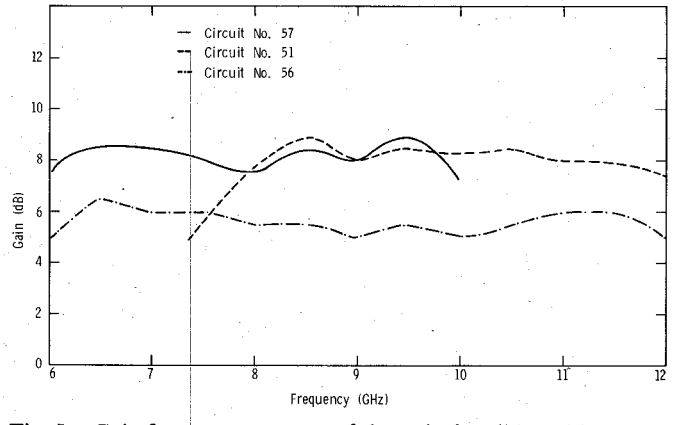


Fig. 5. Gain-frequency response of three single-cell broad-band FET amplifiers.

computer provides the input/output VSWR variations to maintain a constant gain and compensate for the intrinsic gain variation of the FET, as discussed earlier. In general, the highest gain that can be specified in an amplifier design is that corresponding to the MAG of the FET at the highest frequency of interest. This MAG can be computed using the measured S parameters as was shown in Section II.

Fig. 4 shows a photograph of the broad-band microstrip FET amplifier circuit with a topology shown in Fig. 2. A 0.300 by 0.300-in 10-mil-thick alumina is used as the microstrip substrate for both the input and output impedance matching networks. The FET device was mounted upright on a Au-plated copper block sandwiched between the input and output circuits. This device mounting scheme is used for S-parameter measurements to ensure meaningful S-parameter data for the amplifier design. This device–circuit interfacing design also provides a good RF ground plane and allows for easy device and circuit replacement. Minimum thermal resistance was also obtained by mounting the FET directly on the copper block.

Fig. 5 shows the experimental results of three broad-band amplifiers, each optimized for the frequency ranges of 6–10, 8–12, and 6–12 GHz, respectively. Except for higher gain obtained experimentally due to the use of different devices from different slices, these results substantiate the computer calculations shown in Fig. 3. A single-cell FET device with a gate width of 600 μm was used for each of the amplifiers shown in Fig. 5. The 1-dB gain compression point of these amplifier generally exceeds 100 mW.

To further demonstrate the broad-band impedance matching capability of the topology shown in Fig. 2, an amplifier using the same 600-μm gate width FET has also been designed on the computer with a gain of 9 ± 0.3 dB over the frequency range of 2–6 GHz (3:1 bandwidth). Furthermore, an 8–12-GHz amplifier with 9 ± 0.2-dB gain can also be designed using a 1-μm gate length, 300-μm gate width small-signal FET. The line lengths and the impedance levels of the transmission lines can be optimized using the computer routine with the specified gain and ripple. It is thus shown that the unique circuit topology shown in Fig. 2 can be used effectively for FET amplifier design covering different frequencies of operation and/or different FET structures, i.e., gate length, gate width, etc. This is due to the combination of the edge-coupled line section and the short impedance transformers which make it possible to present a very wide range of circuit impedances with desirable reactance slopes to the device for a leveled gain within the frequency band of the amplifier.

IV. Multistage FET Amplifiers

To obtain higher gain in an amplifier, several stages must be cascaded. Either a single-ended or a balanced amplifier configuration can be used. The implementation of the single-ended design requires an appropriate sloped passband insertion-loss function for the interstage networks to produce an amplifier with overall gain flatness [10]. This is especially true for amplifiers designed for wide-band operation. Since the individual stages have significant input/output VSWR variations, as was shown in Section III, additional alignment work will be necessary to minimize the gain variations when several single-ended stages are cascaded. On the other hand, the balanced approach using 90° 3-dB hybrids can be used with the construction of individual stages, that can be easily cascaded with minimum gain variations due to the interstage isolation. Unfortunately, twice as many FET's will be needed as compared with the single-ended approach. In addition, the quadrature hybrids also introduce additional circuit losses. For an amplifier design with a bandwidth of $\sim$ 10 percent it appears to be more attractive to use the single-ended approach, since the individual stages can be designed for minimum VSWR's. Gain variations due to interstage mismatches can thus be avoided. In this section the microstrip circuit development of an X-band 1-W 22-dB-gain GaAs FET amplifier will be described.

The FET power amplifier is to be designed as a driver amplifier operating in the 9.2–9.8-GHz frequency band. Prior to the final integration of the multistage FET amplifier, FET's with various gate widths are tuned for maximum gain at the required RF input levels under optimum bias conditions. Again, the circuit shown in Fig. 2 was used for this purpose with appropriate modifications for the impedance level, line lengths, etc., to account for the different gate widths of the FET's used in different stages. To handle the increased output-power requirement for the power amplifier stage(s), a proportionately larger gate width device was used. Single-, two-, and three-cell

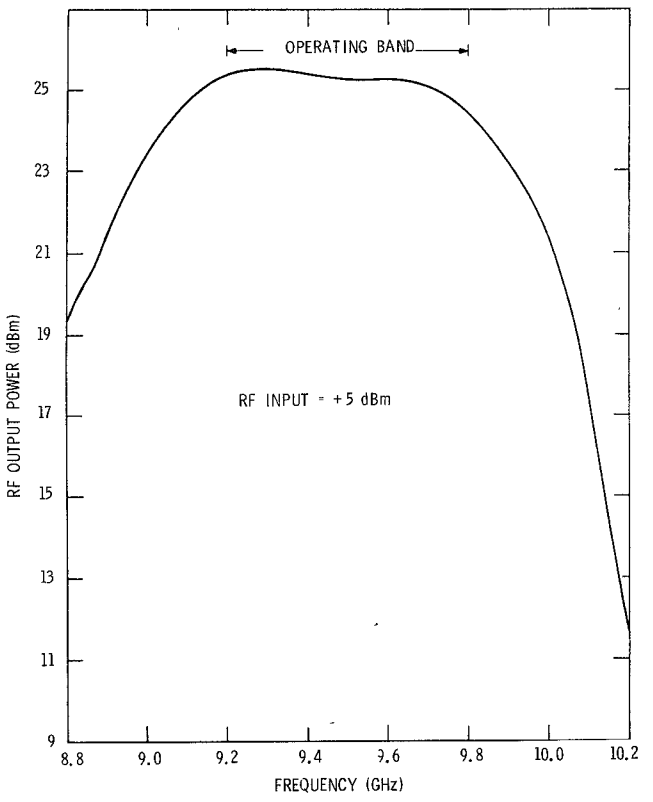


Fig. 6. Frequency response of a three-stage FET amplifier.

FET's are used for the first, second, and third stages, respectively, for a three-stage amplifier. The use of increasingly larger gate width devices for higher power stages not only increases the reliability, but also enhances the linearity of the amplifier.

The amplifier cascading was achieved by removing the input/output OSM connectors used for testing the individual stage. Three stages were then cascaded by bonding a gold strap between the input and output transmission lines. Each of the amplifier stages was then screwed down to the amplifier housing from the bottom side. The bias networks were provided on each side of the amplifier with a removable circuit board. Two bias pins are provided for the gate and drain dc supplies. Fig. 6 shows the output-power frequency response of this amplifier with an RF input power of +5 dBm. An output power (CW) of 360 mW was achieved with a gain of 20.5 dB at 9.3 GHz. A gain of 20 ± 0.5 dB was obtained over the frequency range from 9.1 to 9.8 GHz. The design 1-dB bandwidth was 600 MHz (9.2–9.8 GHz). The 3-dB bandwidth is 1 GHz (8.9–9.9 GHz).

To achieve an output power of 1 W, a fourth stage with a four-cell FET (2400-μm gate width) was added to the three-stage amplifier. Fig. 7 shows the microwave performance of this amplifier. 1 W of output power was obtained with 22-dB gain at 9.5 GHz. The 1-dB design bandwidth was also 600 MHz (9.2–9.8 GHz). The small-signal linear gain was 24 dB at 9.5 GHz. A 3-dB bandwidth of 1.1 GHz (9.1–10.2 GHz) can be obtained.

Third-order intermodulation distortion was measured for the three- and four-stage amplifiers by injecting two

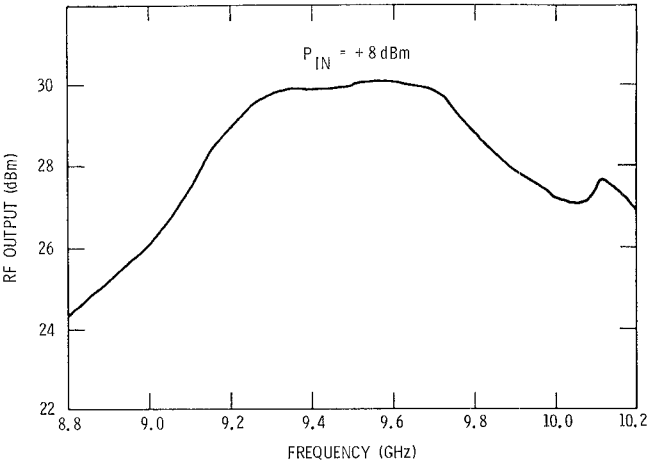


Fig. 7. Frequency response of a four-stage FET amplifier.

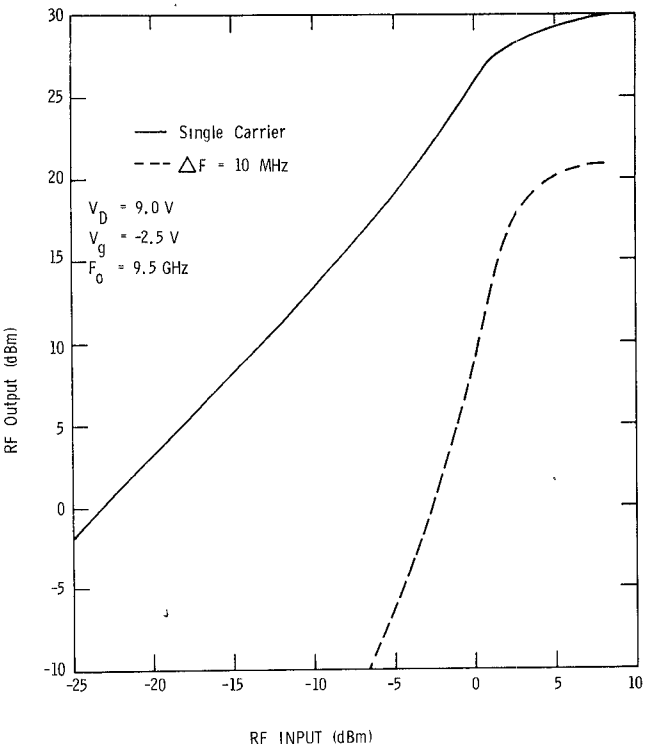


Fig. 8. Third-order intermodulation product versus input level at band center of a four-stage FET amplifier.

equal amplitude signals separated in frequency by 10–50 MHz and located at the band edges and at band center. The input level of the two signals was increased from −20 to +8 dBm while recording the amplitude of the third-order intermodulation product. Fig. 8 shows the fundamental signal output and the third-order intermodulation product versus the input level at the band center for the four-stage amplifier. From these measurements it can be shown that 1) the third-order distortion is not sensitive to the frequency separation of the two input signals, and 2) the third-order distortion of the FET amplifier is essentially independent of frequency within the amplifier passband. The output power was typically 20–25 dBm at a third-order intermodulation level of −20 dB.

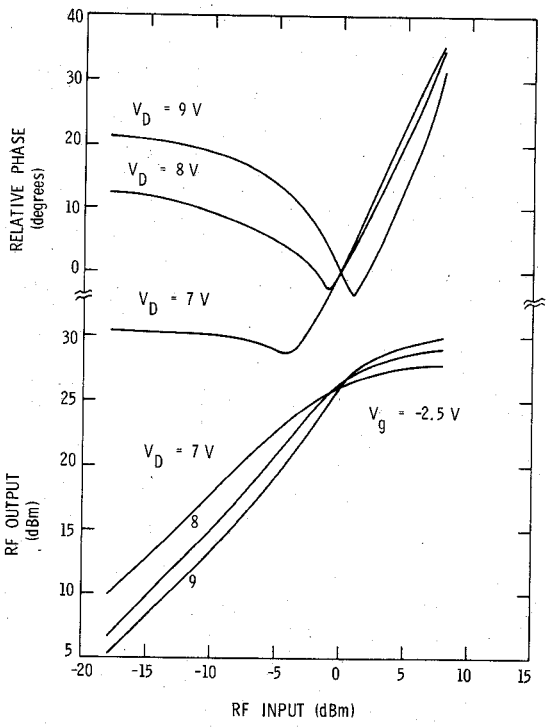


Fig. 9. AM-to-PM conversion and the gain compression characteristics of a four-stage FET amplifier.

AM-to-PM conversion measurements were also performed on the single-stage and multistage FET amplifiers. It is generally observed that AM-to-PM conversion is essentially negligible in the small-signal linear region. For a single-stage amplifier the conversion factor generally remains below 2°/dB even at output-power saturation. Fig. 9 shows the AM-to-PM conversion of the 1-W four-stage amplifier. Also shown in the figure are the input/output curves at three different supply voltages. The insertion phase was measured at 9.5 GHz and was normalized at a nominal input power of 0 dBm. From Fig. 9 it is seen that the maximum AM-to-PM conversion is about 4°/dB, which occurs beyond the 1-dB gain compression point. It is interesting to note that in the small-signal linear region the higher the supply voltage, the lower the gain. This is not too surprising, since each stage of the amplifier chain was tuned for maximum output power rather than maximum linear gain at a drain voltage corresponding to the highest supply voltage shown, i.e., 9 V.

The small-signal noise figure of the three-stage FET amplifier was measured to be in the range of 13–15 dB. Considering that the amplifier was not tuned for minimum noise figure (especially the first stage), the noise figure performance was still superior to that of any other solid-state microwave amplifier with comparable output power and gain.

To demonstrate the feasibility of using the FET amplifier as a driver amplifier, a single-stage *X*-band IMPATT amplifier was used as the output stage in a four-stage hybrid FET/IMPATT amplifier shown in Fig. 10. Fig. 11 shows the output-power frequency response of this amplifier.

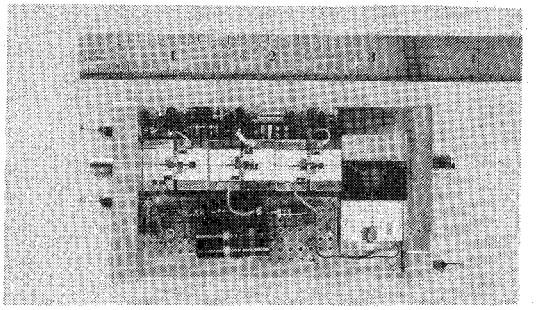


Fig. 10. A photograph of a FET/IMPATT hybrid amplifier.

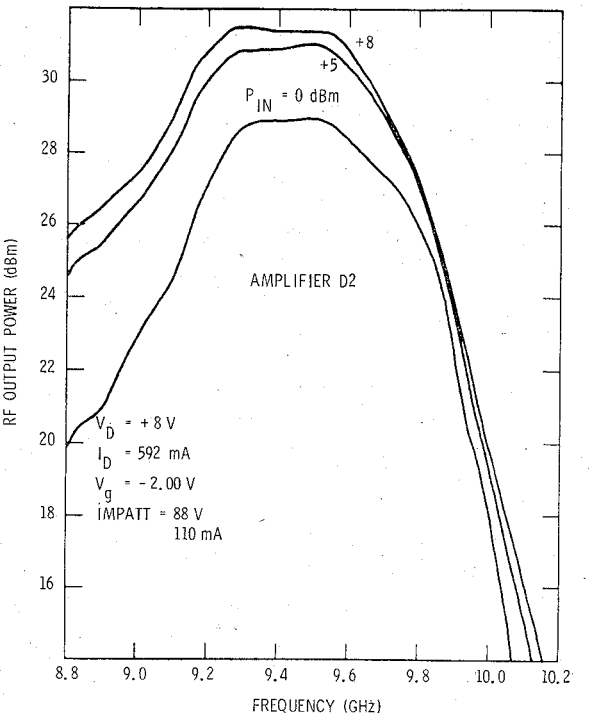


Fig. 11. Output power verses frequency response of the hybrid FET/IMPATT amplifier shown in Fig. 10.

An output power of 1.2 W with 26-dB gain was obtained at 9.5 GHz. The 3-dB design bandwidth is 700 MHz (9.1–9.8 GHz).

Third-order intermodulation measured with this hybrid amplifier indicates a 5–10-dB degradation in the nonlinear distortion for RF input levels between −20 and 0 dBm. This is to be expected since the highly nonlinear avalanche process of the IMPATT diode will undoubtedly add to the third-order distortion even under medium signal conditions.

The degradation of the noise performance due to the IMPATT stage was also measured. In general, a 3–4-dB increase in the small-signal noise figure was observed. This is in close agreement with a prediction based on a theoretical calculation using the gains of the FET and the IMPATT amplifiers and the estimated noise figure of the IMPATT stage (~ 35 dB).

With the use of a high-power Read diode amplifier as the output stage, it is possible to design a hybrid amplifier

having an output power of 5–10 W, while still having the desirable characteristics of low noise and low distortion.

V. Conclusions

The feasibility of using state-of-the-art power GaAs FET devices in the design of power amplifiers in the 6–12-GHz frequency band has been demonstrated. A unique circuit topology incorporating an edge-coupled transmission line section for input/output dc blocking has been described. This circuit topology has been shown to be capable of wide-band impedance matching for FET structures with different gate widths and different frequency ranges of operation. The measured S parameters together with this circuit topology have been used in conjunction with a computer-aided design technique to fabricate three single-stage amplifiers covering the frequency ranges of 6–10, 8–12, and 6–12 GHz. It was also shown that 1 W of CW output power can be obtained with 22-dB gain with a single-ended amplifier design. Microwave performance characteristics such as intermodulation distortion, AM-to-PM conversion, and noise figure were also presented.

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References

[1] H. C. Huang, I. Drukier, R. L. Camisa, S. T. Jolly, J. Goel, and S. Y. Narayan, "GaAs MESFET performance," *Technical Digest*, pp. 235–237, 1975 International Electron Device Meeting.
[2] H. M. Macksey, R. L. Adams, D. N. McQuiddy, and W. R. Wisseman, "*X*-band performance of GaAs power FETs," *Electron. Lett.*, vol. 12, pp. 54–56, Jan. 22, 1976.
[3] R. L. Camisa, J. Goel, and I. Drukier, "GaAs MESFET linear power amplifier stage giving 1 W," *Electron. Lett.*, vol. 11, pp. 572–573, Nov. 27, 1975.
[4] F. N. Sechi and R. W. Paglione, "High-gain 1 W FET amplifier operating in *G*-band," *Digest of Technical Papers*, pp. 162–163, 1976 IEEE International Solid-State Circuits Conference.
[5] C. A. Liechti and R. L. Tillman, "Design and performance of microwave amplifiers with GaAs Schottky-gate field-effect transistors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 510–517, May 1974.
[6] W. H. Ku, M. E. Mokari-Bolhassan, W. C. Peterson, A. F. Podell, and B. R. Kendall, "Microwave octave-band GaAs FET amplifiers," in *IEEE Int. Microwave Symp. Dig. Tech. Papers*, 1975, pp. 69–72.
[7] H. T. Yuan, J. B. Kruger, and Y. S. Wu, "*X*-band silicon power transistor," in *IEEE Int. Microwave Symp. Dig. Tech. Papers*, 1975, pp. 73–75.
[8] H. Q. Tserng, D. N. McQuiddy, and W. R. Wisseman, "*X*-band MIC GaAs IMPATT amplifier module," *J. Solid-State Circuits*, vol. SC-10, pp. 32–39, Feb. 1975.
[9] H. Q. Tserng and D. N. McQuiddy, "*Ku*-band MIC GaAs IMPATT amplifier modules," *IEEE Int. Solid-State Circuits Conf. Digest Tech. Papers*, pp. 78–79, Feb. 1976.
[10] D. J. Mellor and J. G. Linvill, "Synthesis of interstage networks of prescribed gain versus frequency slopes," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 1013–1020, Dec. 1975.

Design, Fabrication, and Evaluation of BARITT Devices for Doppler System Applications

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Abstract—**The properties of BARITT devices and their application in self-mixing Doppler systems are presented. A detailed comparison with IMPATT and Gunn devices indicates that the BARITT is superior in this particular application in many respects, particularly when prime power requirements are important. It is shown that, even though the BARITT device will not compete with existing devices with regard to power output and efficiency, it is the best available device for self-mixed Doppler radar applications and therefore should find wide usage in such applications. Simplified design criteria for BARITT devices are given and fabrication procedures for *X*-band devices with different operating voltages are described.**

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I. Introduction

THE principle of operation of the *bar*rier *i*njection *t*ransit *t*ime (BARITT) device was first proposed by Shockley [1] in 1954. Recently, the first operational BARITT device was reported [2]. Since then, both theoretical and experimental data regarding small-signal as well as large-signal characteristics of the device have been reported by various authors [3]–[7]. In spite of the fact that the BARITT device is inherently a low-power and low-efficiency device, it is found to be a superior device in self-mixed doppler radar applications as compared to IMPATT and Gunn devices, and therefore should be a very useful device in these applications.